address directly, or whether they point to another 4-digit field which contains the required address in relative address format but not aligned to a boundary.

The instruction contains the values of the field in inverse form; the interpretation is

$\overline{IDA}$ = 1 indicates direct addressing for A
$\overline{IDA}$ = 0 indicates indirect addressing for A

and similarly for B. The operation is explained further in Section 3.6.

3.6 *Address Computation*

3.6.1 Operand Relative Address: The relative address of the A Operand is evaluated in two stages as follows:

First, if indirection is specified ($\overline{IDA}$ = 0), the A field in the instruction (PA, A3, A2, A1, A0 and AC) is used to fetch the four byte field containing the indirect address, which is then used in place of the A field.

Second, if indexing is specified (IA ≠ 0), the contents of the specified index register are added.

If extended indexing is not specified ($\overline{EIX}$ = 1), the addition is performed modulo 10000.

If extended indexing is specified ($\overline{EIX}$ = 0), the addition is performed modulo 80000.

3.6.2 A Operand Address Marker, ac: The address marker of the A operand, ac, is evaluated in two stages in parallel with the evaluation of the operand relative address as follows:

First, if indirection is specified ($\overline{IDA}$ = 0), bit 7 of byte A+3 (of the indirect address field) is fetched and used in place of the AC field.

Second, if indexing is specified (IA ≠ 0) and extended indexing also is specified, bit 7 of the least significant byte of the specified index register is combined (logical OR) with the AC field to generate the address marker.

3.6.3 A Operand Absolute Address: If ac = 0, the A operand is in Partition and the A operand absolute address is formed by adding the A operand relative address to the partition base address

If ac = 1, the A operand is in Common and the A operand absolute address is formed by adding the A operand relative address to the Common base address (3000).

3.6.4 B Operand Address: The B operand address is formed in a similar manner using the PB, B3, B2, B1, B0 and BC fields in conjunction with IDB and IB.

3.7 *Instruction Set*

	Mnemonic		Instruction Name	Function Code	
Computational Instructions	A		Add		4
	S		Subtract		7
	M		Multiply		6
	D		Divide		5
	C		Compare		14
	IC	*	Indirect Length Compare		30
	–		Logical Instructions:	LA	20
	AND	*	– And	3	
	OR	*	– Or	1	
	NEQ	*	– Not Equivalent	2	
Address Arithmetic Instructions	MA		Move Address		3
	–		Modify Address Instructions:	LA	2
	AAI		– Add Address Immediate	0	
	AA		– Add Address	1	
	SAI	*	– Subtract Address Immediate	2	
	SA	*	– Subtract Address	3	
	CA	*	– Compare Address	4	
Data Transfer Instructions	MC		Move Character		8
	IM	*	Indirect Length Move Character		24
	MN		Move Numeric		9
	FN		Form Numeric		13
	X		Exchange		15
	PK	*	Pack		31
	UPK	*	Unpack		29
	E		Edit		12
Control Instructions	B		Branch		11
	SM		Set Mode		10
Input/Output Instructions	R		Read		0
	W		Write		1
	SR	*	Start Read		16
	SW	*	Start Write		17
	TS	*	Test IO Status		18

*New Instructions for System 25

4 Input/Output Operations

4.1 *General:*

System 25 Input/Output normally operates in a strictly synchronous manner in